IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20 (Canceled).

Claim 21 (Previously Presented): A redundancy fuse circuit comprising:

a fuse circuit which stores a first address of a defective cell or a block including the defective cell;

a data latch circuit which latches a second address supplied from a tester in a test mode;

a comparator which compares a third address supplied from the tester with one of the first and second addresses, and replaces the defective cell with a redundancy cell when the third address is coincident with one of the first and second addresses; and

a logic circuit which supplies the first address to the comparator in a normal operation mode and supplies the second address to the comparator in the test mode.

Claim 22 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein each of the first and second addresses is one of a row address and a column address.

Claim 23 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the first address is the same as the second address.

Claim 24 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the logic circuit supplies one of the first and second addresses to the comparator based on a test signal.

Claim 25 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the fuse circuit has a fuse device that is cut by a laser.

Claim 26 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the fuse circuit has an electrical fuse device.

Claim 27 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the redundancy fuse circuit is included in a semiconductor memory.

Claim 28 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the redundancy fuse circuit is included in a semiconductor memory which is included in an integrated system.

Claim 29 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the redundancy fuse circuit is included in a memory embedded microcomputer.

Claim 30 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the redundancy fuse circuit is included in a memory embedded microcomputer which is included in an integrated system.

Claim 31 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the redundancy fuse circuit is included in a semiconductor integrated circuit.

Claim 32 (Previously Presented): The redundancy fuse circuit according to claim 21, wherein the redundancy fuse circuit is included in a semiconductor integrated circuit which is included in an integrated system.

Claim 33 (Currently Amended): A method of testing a redundancy fuse circuit, comprising:

latching a defective address to a data latch circuit;

comparing an input address from a tester with the defective address;

replacing a defective cell with a redundancy cell when the input address is coincident with the defective address;

executing a test on the redundancy cell; and

programming the defective address to a fuse circuit after the test, wherein the defective address is programmed to a fuse device that is cut by a laser.

Claim 34 (Previously Presented): The method according to claim 33, wherein the defective address is programmed when the redundancy cell is not defective.

Claim 35 (Previously Presented): The method according to claim 33, wherein the defective address is not programmed when the redundancy cell is defective.

Claim 36 (Previously Presented): The method according to claim 33, wherein the defective address is a row address.

Claim 37 (Previously Presented): The method according to claim 33, wherein the defective address is a column address.

Claims 38-39 (Canceled).

Claim 40 (Previously Presented): The method according to claim 33, wherein the input address is a test address.